AMENDMENTS TO THE CLAIMS

Claims 1-8. (Cancelled).

9. (Currently Amended) A memory device comprising:

a substrate;

a gate stack pair comprising two gate stacks formed on the substrate; a conductive contact between the two gate stacks and in contact with a doped region of the substrate;

a pair of vertical oxide spacers adjacent to each gate stack of said gate stack pair;

a respective nitride layer overlaying and in contact with each said vertical oxide spacer and a top layer of each said gate stack, wherein neither of said nitride layers extends to overlay said doped region and a portion of each said nitride layer is situated between respective vertical oxide spacers; and

a respective dielectric layer overlaying each said nitride layer, the dielectric layer being spaced from each said vertical oxide spacer by said nitride layer such that said dielectric layer is not in direct contact with said vertical oxide layer,

wherein the pair of vertical oxide spacers [[are]] is partially etched back and the respective nitride layers are of a thickness sufficient to fill the etched back portion of a respective one of the pair of vertical oxide spacers.

10. (Previously Presented) The memory device of claim 9, wherein each gate stack of said gate stack pair comprises a floating gate and a control gate.

11. (Previously Presented) The memory device of claim 9, wherein each said vertical oxide spacer is between about 50Å and about 300Å in thickness.

12. (Previously Presented) The memory device of claim 9, wherein each said vertical oxide spacer is about 100Å and about 200Å in thickness.

13. (Previously Presented) The memory device of claim 9, wherein each said respective nitride layer has a thickness equal to about one half the width of each said vertical oxide spacer.

Claims 14-65. (Cancelled).

66. (Previously Presented) The memory device of claim 9, wherein the dielectric layer comprises borophosphosilicate glass.

67. (Previously Presented) The memory device of claim 9, wherein a portion of said nitride layer is in direct contact with a metal layer situated between respective vertical oxide spacers.

68. (Previously Presented) The memory device of claim 9, wherein the respective vertical oxide spacers comprise a top portion and a bottom portion, the bottom portion being nearer to the substrate than the top portion, and a portion of said nitride layer between respective vertical oxide spacers extends below the top portion of the respective vertical oxide spacers.

69. (Previously Presented) The memory device of claim 9, wherein the gate stack is configured such that a cross section taken parallel to a surface of the substrate comprises a first portion of the nitride layer, a portion of a first vertical oxide spacer, a second portion of the nitride layer, a portion of a second vertical oxide spacer, and a third portion of the nitride layer.

70. (Previously Presented) A memory device, comprising:

a substrate comprising a doped region;

first and second gate stacks on a surface of the substrate;

a conductive contact between the first and second gate stacks and in electrical contact with the doped region;

first and second vertical oxide spacers on opposite sides of the first gate stack;

third and fourth vertical oxide spacers on opposite sides of the second gate stack;

a first nitride layer overlaying and in contact with the first and second vertical oxide spacers, wherein a portion of the first nitride layer extends between the first and second vertical oxide spacers;

a second nitride layer overlaying and in contact with the third and forth vertical oxide spacers, wherein a portion of the second nitride layer extends between the third and fourth vertical oxide spacers; and

a dielectric material over the first and second gate stacks, wherein the dielectric material is spaced from the vertical oxide spacers by the nitride layer such that the dielectric layer is not in direct contact with the vertical oxide spacers,

wherein the first, second, third and fourth vertical oxide spacers are partially etched back and the first and second nitride layers are of a thickness sufficient to fill the etched back portion of a respective one of the vertical oxide spacers.

71. (Previously Presented) The memory device of claim 70, wherein the portion of the first nitride layer between the first and second vertical oxide spacers is in direct contact with a metal layer of the gate stack.

72. (Previously Presented) The memory device of claim 70, wherein the first and second vertical oxide spacers each comprise a top surface and a bottom surface, the bottom surface being nearer to the substrate than the top surface, and the portion of the first nitride layer between the first and second vertical oxide spacers extends below the top surface of the first and second vertical oxide spacers.

73. (Previously Presented) The memory device of claim 72, wherein the third and fourth vertical oxide spacers each comprise a top surface and a bottom surface, the bottom surface being nearer to the substrate than the top surface, and the portion of the second nitride layer between the third and fourth vertical oxide spacers extends below the top surface of the third and fourth vertical oxide spacers.

74. (Previously Presented) The memory device of claim 70, wherein the memory device is configured such that a cross section taken parallel to the top surface of the substrate comprises a first portion of the first nitride layer, a portion of a first vertical oxide spacer, a second portion of the first nitride layer, a portion of a second vertical oxide spacer, and a third portion of the first nitride layer.

75. (Previously Presented) The memory device of claim 70, wherein a lower surface of the first nitride layer laterally between the first and second vertical oxide spacers is situated below an uppermost surface of the first vertical oxide spacer.

76. (Previously Presented) The memory device of claim 70, wherein the nitride layers do not extend to overlay the doped region.

Claims 77-79. (Cancelled).